

**STRUCTURE FOR AND METHOD OF FABRICATING
A HIGH-MOBILITY FIELD-EFFECT TRANSISTOR**

[0001] This invention was made with Government support under contract number N6601-00-C-8086 awarded by DARPA. The Government has certain rights in this invention.

CROSS REFERENCE TO RELATED APPLICATIONS

[0002] This application relates to commonly owned, co-pending U.S. Patent Application No. _____ (U.S. Attorney Docket No. YOR920030389US1 (16956)) entitled ULTRA HIGH-SPEED SI/SIGE MODULATION-DOPED FIELD EFFECT TRANSISTORS ON ULTRA THIN SOI/SGOI SUBSTRATE, filed August 29, 2003, the whole contents and subject matter of which is incorporated by reference as if fully set forth herein.

BACKGROUND OF THE INVENTION

Field of the Invention

[0003] The present invention relates to semiconductors and transistors and more particularly to Si/SiGe strained-layer field-effect transistors.

Description of the Prior Art

[0004] Si/SiGe strained layer heterostructures are interesting devices for future high-performance microelectronics applications. In particular, tensile-strained Si on relaxed SiGe MOSFETs have been proposed for advanced CMOS applications, while Si/SiGe modulation-doped field-effect transistors (MODFETs) are of interest for advanced communications applications. Field-effect transistors based upon Si/SiGe strained layers have the common feature that they rely on enhanced mobility to achieve performance improvement. This is especially true for tensile-strained Si on relaxed SiGe MODFETs which can have mobility

enhancement factors of 3-5 times for electrons as described in the reference to K. Ismail, entitled "Si/SiGe high-speed field-effect transistors," *Tech. Dig. Int. Electron Devices Meet.*, 509 (1995) (herein incorporated by reference) and for compressive-strained Ge on relaxed SiGe MODFETs which have hole mobility over 10 times higher than bulk Si MOSFETs as described in the reference to S. J. Koester, R. Hammond, J. O. Chu, entitled "Extremely high transconductance Ge/Si_{0.4}Ge_{0.6} p-MODFET's grown by UHV-CVD," *IEEE Elect. Dev. Lett.* 21, 110 (2000) (herein incorporated by reference).

[0005] However, in order to make a high-performance FET, device design factors in addition to mobility must be considered. In particular, control of short-channel effects is a serious issue for devices with very short gate lengths as recognized by Q. C. Ouyang, S. J. Koester, J. O. Chu, A. Grill, S. Subbanna, and D. A. Herman Jr., at the International Conference on Simulation of Semiconductor Processes and Devices, Kobe, Japan, Sep. 4-6, 2002. In Si MOSFETs, short-channel effects are generally controlled through counter-doping, *i.e.*, introducing carriers of the opposite type into the body of the device in order to maintain a high built-in potential between the source and drain p/n junctions. In Si MOSFETs, counter doping is generally introduced by ion implantation directly through the active area of the device.

[0006] As for SiGe MODFETs, however, implantation of dopants through the active device area can seriously degrade the mobility. The mobility degradation occurs because the trailing edge of the implant profile intersects the high-mobility channel. Since impurity concentrations as low as 10^{15} cm^{-2} can degrade the mobility, even implants with peak concentrations well below the channel region cannot be used. Therefore, it is essential in SiGe MODFETs that the channel region be completely free of implanted impurities in order to maintain the high mobility. An example of the deleterious effect of ion implantation through a Si/SiGe n-channel MODFET structure is shown in the plot of Figure 1(a) illustrating curves 15 showing decreased electron mobility with implant impurities present as compared to the curves 12 showing no implant impurities present.

[0007] One possible option for MODFETs is simply to eliminate the counter-doping, a practice common in III-V devices. However, unlike III-V devices, where high band-gap barrier layers can reduce parallel conduction, the SiGe barrier layers do not provide this opportunity. A demonstration of the need for counter-doping in Si/SiGe n-MODFETs is shown in the plot of Figure 1(b), which shows experimental data of a scaled Si/SiGe n-MODFET with no p-well along with physical simulations of a very similar device with p-type counter doping. The device without counter doping (p-well) shows severe short-channel effects and large source/drain leakage current, while the simulations show that with the proper p-well doping the same device would exhibit near ideal subthreshold behavior.

[0008] To date, no method of introducing counter doping into SiGe MODFETs have been explicitly suggested. However, the concept of incorporating the doping via an *in situ* doping process has been proposed and implemented using tensile-strained Si surface channel MOSFETs in the reference to K. Rim, J. L. Hoyt, J. F. Gibbons, entitled "Fabrication and analysis of deep submicron strained-Si N-MOSFET's," *IEEE Trans. on Elect. Dev.* 47, 1406 (2000). However, this technique is not applicable for a layer structure grown on a pre-fabricated relaxed SiGe substrate where the regrown layer structure needs to be kept thin, since the doping is only incorporated in the epitaxially regrown layer, and therefore the underlying substrate could still act as a leakage path. A good example of this situation occurs for a MODFET fabricated on a buried insulating layer, where the typical fabrication scheme would be to first produce a wafer of relaxed SiGe on insulator, and then regrow the MODFET layer structure on top. In this situation, *in situ* doping of the p-well during growth would still leave the original SiGe substrate undoped. *In situ* doping is also a problem for p-channel SiGe MODFETs, since the counter doping would have to be n-type, and many common n-type dopants have a high surface affinity during growth, segregating to the surface and causing unintentional dopant incorporation into the channel layer.

[0009] It would thus be highly desirable to produce a high-mobility semiconductor layer structure and field-effect transistor exhibiting a high-mobility conducting channel, while at the

same time, maintaining counter doping to control deleterious short-channel effects. It would also be highly desirable to provide a method of fabricating such a layer structure and transistor.

SUMMARY OF THE INVENTION

[0010] It is thus an object of the present invention to provide a high-mobility semiconductor layer structure and field-effect transistor that includes a high-mobility conducting channel, while at the same time, maintaining counter doping to control deleterious short-channel effects.

[0011] According to one embodiment of the invention, there is provided a semiconductor layer structure comprising: a relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer, a portion of which is doped p-type; a bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer on top of the relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer, where the Ge concentration, z , is such that said bottom buffer layer is substantially lattice-matched to said relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer; a tensile-strained Si quantum well layer on top of the bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer; a top $\text{Si}_{1-m}\text{Ge}_m$ buffer layer on top of the tensile-strained Si quantum well layer; and a tensile-strained Si cap layer on top of the top $\text{Si}_{1-m}\text{Ge}_m$ buffer layer.

[0012] In a further embodiment, the relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer has a Ge concentration, x and relaxation, r such that the in-plane lattice constant is 0.8-2.4% larger than that of bulk Si, and includes a p-type doped portion with a concentration ranging between 10^{15} cm^{-3} and 10^{19} cm^{-3} ; and said bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer has thickness ranging from 2 nm to 50 nm, and said tensile-strained Si quantum well layer, and said top $\text{Si}_{1-m}\text{Ge}_m$ buffer layer has thickness ranging from 2 nm to 20 nm.

[0013] In a further embodiment, a thin $\text{Si}_{1-y}\text{Ge}_y$ layer may be interposed between the top of the relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer and bottom buffer layer having with a Ge concentration, y , in the range of 0 to 20%, and thickness in the range of 1 to 5 nm.

[0014] In a further embodiment, said relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer may be on a buried insulating layer, said relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer having a thickness of 5 to 100 nm.

[0015] It is another object of the present invention to provide a method of fabricating a high-mobility semiconductor layer structure and field-effect transistor that includes a high-mobility conducting channel wherein the method allows the counter doping to be formed using a standard technique such as ion implantation or in situ doping, and further allows the high-mobility channel to be in close proximity to the counter doping without degradation of the mobility.

[0016] Advantageously, a high-performance n-MODFET transistor device may be formed by additionally providing an insulating gate dielectric on top of the Si cap layer; a gate electrode located on top of the insulating gate dielectric; and, n-type source and drain contact regions located on either side of said gate electrode that extend from a surface of the multi-layer structure into the p-type doped portion of the relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer. It is understood that p-type MODFET devices may be formed according to the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Further features, aspects and advantages of the apparatus and methods of the present invention will become better understood with regard to the following description, appended claims, and accompanying drawings where:

[0018] Figure 1(a) is a graph depicting the mobility vs. temperature for an n-type modulation-doped layer structure with and without p-well implantation.

[0019] Figure 1(b) are experimental I_d vs. V_{gs} curves at $V_{ds} = 0.2$ and 1 V for SiGe n-MODFETs without p-well doping; and simulated I_d vs. V_{gs} curves at $V_{ds} = 0.2$ and 1 V for SiGe n-MODFETs with p-well doping;

[0020] Figure 2 is a schematic cross-sectional view of an undoped tensile-strained Si quantum well layer structure with p-type doped body;

[0021] Figure 3 is a schematic cross-sectional view of a tensile-strained Si quantum well layer structure with n-type modulation doping and p-type doped body;

[0022] Figure 4 is a schematic cross-sectional view of a tensile-strained Si quantum well layer structure with n-type modulation doping, p-type doped body and a SiGe interposer layer;

[0023] Figure 5 is a schematic cross-sectional view of a tensile-strained Si quantum well layer structure with n-type modulation doping, and p-type doped body on a buried insulating layer.

[0024] Figure 6 is a schematic cross-sectional view of a compressive-strained SiGe quantum well layer structure with p-type modulation doping and n-type doped body;

[0025] Figure 7 is a schematic cross-sectional view of an n-type field-effect transistor with an undoped tensile-strained Si quantum well layer structure, n-type modulation doping, p-type doped body and self-aligned source/drain contacts;

[0026] Figure 8 is a schematic cross-sectional view of an n-type field-effect transistor with a tensile-strained Si quantum well layer structure, n-type modulation doping and p-type doped body;

[0027] Figure 9 depicts a process sequence for growing the layer structure shown in Figure 4; and,

[0028] Figures 10(a)-10(c) depict experimental data of an n-MODFET layer structure with a p-type implanted SiGe substrate.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0029] Figure 2 is a schematic cross-sectional view of an undoped tensile-strained Si quantum well layer structure with p-type doped body according to a preferred embodiment of the invention. The layer structure comprises a relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer 10, where a portion of this layer is doped p-type. The possible range of p-type dopant concentration is between 10^{15} and 10^{19} cm^{-3} , and in the preferred embodiment the concentration is ideally between 10^{16} and 10^{18} cm^{-3} . In one embodiment said p-type doped portion may be a top portion 11 of the relaxed layer 10 as shown in Figure 2, however, the whole or a substantial portion of the relaxed layer 10 may be doped p-type. The Ge concentration, x , and relaxation, r , of layer 10 should be such that the in-plane lattice constant is 0.8-2.4% larger than that of relaxed Si, with preferred values in the range of 1.2 to 1.8%. On top of this layer is bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 20, where the Ge concentration z , is such that layer 20 is roughly lattice-matched to layer 10. On top of bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 20 is tensile-strained Si layer 30, followed by top $\text{Si}_{1-m}\text{Ge}_m$ buffer layer 40, and optionally, Si cap layer 50. In general, top $\text{Si}_{1-m}\text{Ge}_m$ buffer layer 40, bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 20 and $\text{Si}_{1-x}\text{Ge}_x$ layer 10 are not required to have the same Ge concentration, though in the preferred embodiment, the Ge concentrations of the three layers are about the same. In this embodiment, high mobility in tensile-strained Si layer 30 is maintained because the p-well doping is restricted to the underlying $\text{Si}_{1-x}\text{Ge}_x$ layer 10, separated from the quantum well by bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 20. Ideally, the thickness of bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 20 should be sufficiently thin to allow the p-well doping to effectively control short-channel effects, but thick enough to prevent mobility degradation. The possible range of thickness for bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 20 is from 2 nm to 50 nm, with preferred values of between 10 and 30 nm. Also, in the preferred embodiment, the thickness of tensile-strained Si layer 30 is such that it is less than the critical thickness for misfit dislocation formation at the interface between bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 20 and tensile-strained Si layer 30. Also, in the preferred embodiment, the combined thicknesses of top $\text{Si}_{1-m}\text{Ge}_m$ buffer layer 40 and Si cap layer 50 are no more than 20 nm.

[0030] According to the invention, n-type modulation doping may be incorporated into the layer structure as shown in Figure 3. In particular, n-type modulation doping with a concentration

between 10^{17} and 10^{21} cm^{-2} may be incorporated into either top $\text{Si}_{1-m}\text{Ge}_m$ buffer layer 140 or bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 120, or both, with the provision that at least a portion of each layer immediately adjacent to Si quantum well 130, remain substantially undoped. In this case, bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 120, is split into n-type supply layer 180, and substantially undoped spacer layer 190, and top $\text{Si}_{1-m}\text{Ge}_m$ buffer layer 140, is divided into n-type supply layer 160, and substantially undoped spacer layer 170. The thickness of undoped spacer layers 170 and 190 must be at least 0.5 nm, to ensure that the high mobility is maintained in Si quantum well 130. In the preferred embodiment, the n-type doping in n-type supply layers 160 or 180 or both has concentration in the range of 10^{18} to 10^{20} cm^{-3} . Also, the preferred thickness of doped n-type supply layer 160 is in the range from 5 nm to 15 nm, and the preferred thickness of undoped spacer layer 170 is in the range from 2 nm to 8 nm. The thicknesses of layers 160 and 170 should also be such that their combined thickness is no more than 20 nm.

[0031] Figure 4 shows a schematic cross-sectional view of another embodiment of the invention where a thin interposer layer 220 of $\text{Si}_{1-y}\text{Ge}_y$, where $y < 20\%$, is placed between relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer 210 and $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 230. In Figure 4, layers 240, 250 and 260 correspond respectively to layers 130, 140 and 150 of Figure 3. The interposer layer 220 may help to getter contamination, mainly C and O, before the subsequent layers 230-280 are grown on top of layer 210. By reducing contamination, the interposer layer may permit Si quantum well 240 to be closer to the p-type doped region of relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer 210, thereby allowing better short-channel control, while still maintaining high mobility. In the preferred embodiment, the thickness of interposer layer 220 should be between 1 nm and 5 nm, and the Ge concentration, y , is less than 10%.

[0032] The layer structures described herein may additionally incorporate a buried insulating layer. As an example, Figure 5 shows one embodiment comprising from bottom to top, an Si substrate 310, and buried insulator layer 320, which in the preferred embodiment, may comprise an oxide, nitride, oxynitride of silicon, and preferably SiO_2 . Next is relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer 330, which can be completely or partially doped p-type. On top of this layer is bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 340, where the Ge concentration z , is such that layer 340 is roughly lattice-matched to layer 330. On top of bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 340 is tensile-strained Si layer 350, followed by top

$\text{Si}_{1-m}\text{Ge}_m$ buffer layer 360, and optionally, Si cap layer 370. In Figure 5, top-side modulation doping is shown, which divides $\text{Si}_{1-m}\text{Ge}_m$ buffer layer 360 into n-type supply layer 380, and substantially undoped spacer layer 390. Though top-side modulation doping is shown Figure 5, layer structures with top and/or bottom, or no modulation doping are also possible. The thin interposer layer of $\text{Si}_{1-y}\text{Ge}_y$, described in Figure 4, may also be utilized in the embodiment illustrated in Figure 5, and would be located between relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer 330 and bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 340. In this embodiment, the preferred range of doping levels, Ge concentrations, strain levels and layer thicknesses are the same as in the previous embodiments.

[0033] The concept of using a buried layer with counter-doping for a tensile-strained Si n-channel heterostructure, may also be applied to a strained p-channel heterostructure. Figure 6 is a schematic cross-sectional view of a strained SiGe quantum well layer structure with p-type modulation doping and n-type doped body according to another embodiment of the invention. In this embodiment, the layer structure is a high-mobility p-channel heterostructure comprising a relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer 410, where the top portion 411 of this layer is doped n-type. It is understood however, that the whole or a substantial portion of the relaxed layer 410 may be doped n-type. The possible range of n-type dopant concentration is between 10^{15} and 10^{19} cm^{-3} , and in the preferred embodiment the concentration is ideally between 10^{16} and 10^{18} cm^{-3} . The Ge concentration, x , and relaxation, r , of layer 410 are such that the in-plane lattice constant is 0-3.2% larger than that of relaxed Si, with preferred values in the range of 1.2% to 2.4%. Formed on top of this layer is bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 420, where the Ge concentration z , is such that layer 420 is roughly lattice-matched to layer 410. On top of layer 420 is strained $\text{Si}_{1-v}\text{Ge}_v$ layer 430, where, $v > z$, such that strained $\text{Si}_{1-v}\text{Ge}_v$ layer 430 is under compressive strain thus forming a quantum well for holes. In the preferred embodiment, $v > z+0.3$. On top of layer 430 is formed top $\text{Si}_{1-m}\text{Ge}_m$ buffer layer 440, and Si cap layer 450. In general, top $\text{Si}_{1-m}\text{Ge}_m$ buffer layer 440, bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 420 and $\text{Si}_{1-x}\text{Ge}_x$ layer 410 are not required to have the same Ge concentration, though in the preferred embodiment, the Ge concentrations of the three layers are about the same. Also, in another embodiment of the invention either $\text{Si}_{1-m}\text{Ge}_m$ buffer layer 440, or Si cap layer 450, but not both, could be omitted from the layer structure, because either of these layers can produce the required band offset to provide confinement of the holes in strained $\text{Si}_{1-v}\text{Ge}_v$ layer 430.

[0034] In Figure 6, p-type modulation doping is incorporated within bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 420. In this case, bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 420, is divided into p-type supply layer 460, and substantially undoped spacer layer 470. The thickness of undoped spacer layer 470 must be at least 0.5 nm, to ensure that the high mobility is maintained in $\text{Si}_{1-y}\text{Ge}_y$ quantum well 430. Similar to layer structures in Figures 2-5, the layer structure in Figure 6 may also include modulation doping in either bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 420 or top $\text{Si}_{1-m}\text{Ge}_m$ buffer layer 440 or both, a buried insulating layer under $\text{Si}_{1-x}\text{Ge}_x$ buffer layer 410, and/or a $\text{Si}_{1-y}\text{Ge}_y$ interposer layer between bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 420, and $\text{Si}_{1-x}\text{Ge}_x$ layer 410. The possible range of thickness for $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 420 is from 2 nm to 50 nm, with preferred values of between 10 and 30 nm. Also, in the preferred embodiment, the thickness of strained $\text{Si}_{1-y}\text{Ge}_y$ layer 430 is such that it is less than the critical thickness for misfit dislocation formation at the interface between bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 420 and strained $\text{Si}_{1-y}\text{Ge}_y$ layer 430, and the combined thicknesses of $\text{Si}_{1-m}\text{Ge}_m$ buffer layer 440 and Si cap layer 450 are no more than 20 nm.

[0035] The current invention additionally comprises field-effect transistors incorporating the layer structures described herein with respect to Figures 2-6. The essential components of the field-effect transistors of the invention are shown in Figure 7, which shows a schematic cross-sectional view of a n-type transistor with a buried p-well region. In its simplest form, the transistor incorporates the layer structure shown in Figure 2, which comprises a relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer 510, having a portion 511 of this layer doped p-type, followed by bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 520, where the Ge concentration z , is such that layer 520 is roughly lattice-matched to layer 510. On top of bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer 520 is tensile-strained Si layer 530, followed by top $\text{Si}_{1-m}\text{Ge}_m$ buffer layer 540, and optionally, Si cap layer 550. The device structure shown in Figure 7 further comprises trench isolation regions 560 that penetrate into relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer 510, a gate dielectric layer 570, a gate electrode 580, and n-type source and drain contact regions 590 that are self-aligned to the gate electrode. Preferably, the gate dielectric layer 570 comprises an oxide, nitride, oxynitride of silicon, and oxides and silicates of Hf, Al, Zr, La, Y, Ta, singly or in combinations, while the gate electrode 580 may comprise polysilicon, polysilicongermanium, or metals such as Pt, Ir, W, Pd, Al, Au, Ni, Cu, Ti, Co and their silicides and germanosilicides, either singly or in combinations. The N-type source and drain contact regions 590 are deep

enough such that they penetrate into but not through the p-type region 511 of relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer 510. Therefore, conduction is blocked between source and drain through relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer 510 due to the presence of back-to-back p-n junctions. High-mobility is maintained since the channel region (tensile-strained Si layer 530) remains substantially undoped.

[0036] In the embodiment of the invention depicted in Figure 7, the gate electrode 580 is isolated from the source and drain by gate dielectric 570. In addition, source and drain contact regions 590 must be overlapped by the gate slightly to ensure continuity between source and drain. In another embodiment of the invention, modulation doping may be used to populate the channel, thus allowing offset source and drain regions. Such an embodiment is shown in Figure 8 which depicts a schematic cross-sectional view of an n-type field-effect transistor with a tensile-strained Si quantum well layer structure, n-type modulation doping and p-type doped body. In this embodiment, the layer structure comprises a relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer 610, the top part of which is doped p-type, followed by bottom $\text{Si}_{1-x}\text{Ge}_x$ buffer layer 620, tensile-strained Si layer 630, undoped $\text{Si}_{1-m}\text{Ge}_m$ spacer layer 640, n-type doped $\text{Si}_{1-m}\text{Ge}_m$ supply layer 650 and, optionally, a Si cap layer 660. The device structure further includes trench isolation regions 670 that penetrate into relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer 610, a Schottky gate electrode 680, and n-type source and drain contact regions 690 that penetrate into the p-type region of relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer 610. In this embodiment, because the modulation-doping populates tensile-strained Si layer 630, the source and drain contacts may be offset from the gate electrode. This enables source and drain contact regions 690 to be farther apart, which in turn, reduces the concentration of p-type doping in relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer 610 required to control short channel effects. Additionally, modulation-doped eliminates the need for a strong forward gate bias, thus reducing the parasitic population of Si cap layer 660. In the embodiment depicted in Figure 8, the Schottky gate electrode 680 is preferably metal, with contact metal having a high work function. Preferred metals for this contact include, but are not limited to: Ir, Pt and Pd. The embodiment depicted in Figure 8 may additionally utilize an insulating gate as in Figure 7, but does not require one.

[0037] The device embodiments shown and described in view of Figures 7 and 8 may additionally incorporate other variations of the layer structure described in Figures 2-6. Specifically, the devices may incorporate a layer structure on a buried insulating layer, as shown

in Figure 5. In this embodiment, the isolation-trenches and the source/drain contact regions would extend down to the buried insulating (e.g. oxide) layer. The buried insulating layer would reduce the capacitance of the source/drain junctions, and provide additional benefit in controlling short-channel effects. The device embodiments depicted may additionally include a p-type field-effect transistor by utilizing the layer structure in Figure 6, and p-type source and drain regions.

[0038] The invention additionally includes a methodology for fabricating the multi-layer structures described in Figures 2-6. One embodiment of the invention shown in Figure 9, depicts a method for fabricating the multi-layer structure described in Figure 4. The method starts with a partially or fully relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer as shown in Figure 9(a). The Ge concentration, x , and relaxation, r , of relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer are such that the in-plane lattice constant is 0.8-2.4% larger than that of relaxed Si. Relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer may be fabricated in a number of ways, but the typical method is to grow a graded SiGe buffer layer on a Si substrate, where the Ge concentration is slowly graded from $x = 0$ to the final Ge concentration, x . Next, as shown in Figure 9(b), the relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer is implanted with a p-type dopant species. In the preferred embodiment, this dopant would include B or In, or a combination of the two. The sample is then annealed to activate the dopants. The annealing may occur at a temperature necessary to properly activate the dopants, and typically range between 700-1100°C. In the next processing the wafer is cleaned to prepare the surface for regrowth. In one embodiment of the invention, the first regrown layer is a thin (*i.e.*, less than 5 nm) interposer or seed $\text{Si}_{1-y}\text{Ge}_y$ layer, as depicted in Figure 9(c), where the Ge concentration, y , is in the range of 0 to 20%. This layer helps to getter contaminants, particularly, C and O, at the regrowth interface so they do not segregate into the subsequent regrown layers. On top of this layer is grown the bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer layer as depicted in Figure 9(d), where the Ge concentration z , is such that this layer is roughly lattice-matched to the relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer. Next, as shown in Figure 9(e), the tensile-strained Si quantum well is grown, followed by a top $\text{Si}_{1-m}\text{Ge}_m$ buffer layer (Figure 9(f)) and, finally, a Si capping layer (Figure 9(h)). In one embodiment of the invention, all of the regrown layers are substantially undoped. In another embodiment of the invention, the layers are grown at a temperature or temperatures in the range of 350 °C to 600 °C.

[0039] In another embodiment of the invention as described herein, modulation-doping may be incorporated in the following way: after growing the tensile-strained Si quantum well as depicted in Figure 9(f), a portion of the top $\text{Si}_{1-m}\text{Ge}_m$ buffer layer is grown such that it is substantially undoped, and has thickness of at least 0.5 nm. Then, a remaining portion of top $\text{Si}_{1-m}\text{Ge}_m$ buffer layer is grown with n-type doping to form n-type supply layer. In the preferred embodiment, the n-type dopant is P, As or Sb. Finally, the Si capping layer is grown, which may or may not include n-type doping. A similar method may be used for doping the bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer n-type, with the provision that the Si quantum well and the region of bottom $\text{Si}_{1-z}\text{Ge}_z$ buffer within 0.5 nm of the Si quantum well must remain substantially undoped.

[0040] In yet another embodiment of the invention, there is utilized a reduced growth temperature for the $\text{Si}_{1-y}\text{Ge}_y$ interposer layer and the $\text{Si}_{1-z}\text{Ge}_z$ bottom buffer layer (Figure 9(c) and 9(d)), in order to prevent three-dimensional growth associated with elastic relaxation. The temperature is then ramped back up to the nominal growth temperature during the growth of the Si quantum well, and for the subsequent layers. In the preferred embodiment, the growth temperature for the $\text{Si}_{1-y}\text{Ge}_y$ interposer layer is between 450°C and 550°C, and the growth temperature for the $\text{Si}_{1-z}\text{Ge}_z$ bottom buffer layer is between about 350°C and 500°C.

[0041] The basic principle of this invention is demonstrated as shown with reference to Figures 10(a)-10(c) which depict experimental data of a MODFET layer structure regrown on a p-well implanted SiGe substrate. Figure 10(a) particularly depicts a secondary ion mass spectroscopy (SIMS) plot of the multi-layer structure with implanted p-well doping, and regrown Si/SiGe modulation-doped quantum well layer structure and Figure 10(b) depicts a corresponding cross-sectional transmission electron micrograph (XTEM) of the multi-layer structure shown in Figure 10(a). As shown in Figures 10(a) and 10(b), the data illustrates that smooth regrowth is obtained by using the technique of reduced growth temperature described hereinabove. Furthermore, the results of Hall measurements show that the p-well doping has minimal impact on the room-temperature mobility as shown in the data depicted in Figure 10(c).

[0042] While the invention has been particularly shown and described with respect to illustrative and preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention that should be limited only by the scope of the appended claims.